passing information contained in said program to said memory;

discerning a failure evidencing an incomplete or incorrect program element in said memory by reprocessing information received in said information transmission; and

executing a predetermined secondary error correction routine in consequence of said step of discerning a failure.

6. The method of claim 5, wherein one of said primary error correction routine and said secondary error correction routine comprises clearing some or all of said memory.

7. The method of claim 5, further comprising the step of placing or replacing data at said memory to complete or correct a program element in consequence of said step of executing a predetermined secondary error correction routine.

8. The method of claim 5, further comprising the step of interrupting a processor in accordance with one of said primary error correction routine and said secondary error correction routine.

9. The method of claim 5, further comprising the steps of:

selecting a value designating an instruction to be executed; and

jumping to a memory location based on said selected value.

10. The method of claim 5, wherein said step of selecting a value comprises computing at least some an address of said memory location.

11. The method of claim 5, further comprising the steps of:

storing history-of-efficiency information; and

instituting or restoring functionality of at least one of said one or more processors based on said stored history of efficiency information.

12. The method of claim 5, wherein said step of discerning a failure comprises comparing information stored at a first memory location to information stored at a second memory location.

13. The method of claim 5, wherein at least one of said first memory location and said second memory location is a dedicated register at said one or more processors.

14. The method of claim 5, wherein said primary error correction routine includes forward error correction and said step of discerning a failure is based on information processed in said step of performing primary error correction.

15. The method of claim 5, wherein said incomplete or incorrect program element in said memory is one of (1) an incomplete or incorrect element of said received program and (2) some or all of a second program.

16. The method of claim 5, further comprising the step of performing forward error correction information to be outputted in or with said program before performing said steps of (1) performing a primary error correction routine and (2) discerning a failure.

17. The method of claim 5, wherein said step of performing a primary error correction routine further comprises selecting program material to be or not to be outputted at said receiver station.

18. The method of claim 5, further comprising selecting program material to be or not to be outputted at said receiver station in accordance with said second error correction routine.

19. The method of claim 5, wherein said program includes one or more of a television program, a radio program, a computer program, and some of a combined medium program.

20. The method of claim 19, further comprising the step of selecting one or more of a program instruction set, intermediate generation set, combining synch command, and data to be processed to present combined medium programming.

21. The method of claim 20, further comprising the step of programming said receiver station with at least some of said primary error correction routine and said secondary error correction routine.

22. The method of claim 21, wherein said step of programming said receiver station comprise:

receiving said at least some of said primary error correction routine and said secondary error correction routine from a remote station;

directing said received at least some of said primary error correction routine and said secondary error correction routine from a remote station to at least one of a register

and a reprogrammable memory operatively connected to said one or more processors; and

storing said at least some of said primary error correction routine and said secondary error correction routine at said at least one of a register and a reprogrammable memory operatively connected to said one or more processors.

23. A method of controlling a receiver station, said receiver station including a receiver, a memory operatively connected to said receiver, and one or more processors operatively connected to said memory, comprising the steps of:

(1) receiving an information transmission at a transmission station;

(2) generating a program; and

(3) transmitting said information transmission containing said program to enable said receiver station to perform a primary error correction routine by processing at least some of said information transmission, discerning a failure evidencing an incomplete or incorrect program element by reprocessing information received in said information transmission, and executing a predetermined secondary error correction routine in consequence of discerning a failure.

24. A method of controlling a receiver station, said receiver station including a receiver, a memory operatively connected to said receiver, and one or more processors operatively connected to said memory, comprising the steps of:

(1) receiving an information transmission to be transmitted;

(2) receiving an instruct signal which is effective to: